What is claimed is:

1. A structure of a multi-gate thin film transistor, comprising:

a polycrystalline silicon layer formed on a substrate having a source region, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region, said polycrystalline silicon layer having geometry selected one from a stair shaped and L-shaped from top view, at least one of said first gate channel and said second gate channel being along a data line direction;

a multi-gate formed on said substrate and intersected with said polycrystalline silicon layer so that said first gate channel and said second gate channel are formed; and

a gate oxide layer formed in between said multi-gate and said polycrystalline silicon layer.

2. The structure of claim 1, wherein said polycrystalline silicon layer is a stair-shaped in geometry from top view with two horizontal sections and one vertical section, said multi-gate comprises a scanning line and a I-shaped gate extension portion, respectively, intersect two of sections of said stair-shaped polycrystalline silicon layer to form said first gate channel and said second gate channel.

3. The structure of claim 1, wherein said polycrystalline silicon layer is a L-shaped in geometry with one horizontal section and one vertical section, and said multi-gate comprises a scanning line and a L-shaped gate extension portion, and both intersect with said vertical section of said L-shaped polycrystalline silicon layer to form said first gate channel and said second gate channel, said source region formed on said horizontal section and said drain region formed on said vertical section.

4. The structure of claim 3, wherein said multi-gate comprises a scanning line and a L-mirror-shaped gate extension portion, and both intersect with said vertical section of said L-shaped polycrystalline silicon layer to form said first gate channel and said

second gate channel, said source region formed on said horizontal section and said drain region formed on said vertical section.

5. The structure of claim 1, wherein said polycrystalline silicon layer is a L-shaped in geometry with one horizontal section and one vertical section, said multi-gate comprises a scanning line and a I-shaped gate extension portion perpendicular to said canning line, intersect, respectively, with said vertical section and horizontal section to form said first gate channel and said second gate channel, said source region formed on said horizontal section and said drain region formed on said vertical section.

6. The structure of claim 1, wherein said polycrystalline silicon layer is a L-shaped in geometry with a first horizontal section and a first vertical section, said multi-gate comprises a scanning line and a L-shaped gate extension portion having a second vertical section and a second horizontal section intersect, respectively, with said first horizontal section and said first vertical section to form said first gate channel and said second gate channel, said source region formed on said first horizontal section and said drain region formed on said first vertical section.

7. The structure of claim 1, further comprising a heavily doped region formed into second doped region to reduce resistance.

8. A structure of a multi-gate thin film transistor, comprising:

a polycrystalline silicon layer formed on a substrate having a source region, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region, further, said polycrystalline silicon layer having a stair shaped in geometry from top view, still, at least one of said first gate channel and said second gate channel being along a data line direction;

a dual-gate formed on said substrate having a scanning line and a I-shaped gate extension portion intersected with said polycrystalline silicon layer so that one of said

first gate channel and said second gate channel along said data direction; and

a gate oxide layer formed in between said multi-gate and said polycrystalline silicon layer.

9. A structure of a multi-gate thin film transistor, comprising:

a polycrystalline silicon layer formed on a substrate having a source region, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region, further, said polycrystalline silicon layer having geometry of L-shaped from top view having a first horizontal section formed with said drain region formed at an ended thereof and a first vertical section formed with said source region at an ended thereof;

a dual-gate formed on said substrate having a scanning line and an extension portion perpendicular to said scanning line, said extension portion being selected one geometry from I shaped, L-shaped, and L-mirror shaped, said dual-gate intersected with said polycrystalline silicon layer so that said first gate channel and said second gate channel are formed and at least one of said first gate channel and said second gate channel being along a data line direction; and

a gate oxide layer formed in between said multi-gate and said polycrystalline silicon layer.

10. The structure of claim 9, wherein said extension portion is L-shaped having a second vertical section and a second horizontal section, said scanning line and said second horizontal section intersect with said first vertical section to form said first gate channel and said second gate channel.

11. The structure of claim 9, wherein said extension portion is I-shaped, said first horizontal section and said first vertical section intersects, respectively, with said extension portion and said scanning line to form said first gate channel and said second

gate channel.

12. The structure of claim 9, wherein said extension portion is L-mirror shaped having a second vertical section and a second horizontal section, said scanning line and said second horizontal section intersect with said first vertical section to form said first gate channel and said second gate channel.

13. The structure of claim 9, wherein said extension portion is L-shaped having a second vertical section and a second horizontal section, said second horizontal section and said second vertical horizontal section intersect with said first vertical section and said first vertical section to form said first gate channel and said second gate channel.